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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,913	07/07/2003	Jun Sumino	67161-066	4870

7590 08/04/2004

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,913	SUMINO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *5-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/07/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/07/2003 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Group I, claims 1-4, in the reply filed 07/07/2004 is acknowledged. The requirement is still deemed proper and is made FINAL.

3. Claims 5-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1 and 2** are rejected under 35 U.S.C. 102(e)(2) as being anticipated by Shimizu et al. U.S. Patent 6,555,427.

Shimizu discloses in Figure 19A and respective portions of the specification a non-volatile semiconductor memory device as claimed.

Referring to **claim 1**, Shimizu discloses a non-volatile semiconductor memory device comprising:

a semiconductor substrate (1) having a main surface provided with two spaced trenches (defined generally by isolation insulators 2);

an isolation insulator (2) filling said trench, said isolation insulator having an upper surface with an end having a curvature (101, as marked by the examiner) protruding toward said semiconductor substrate;

a floating electrode (5-1, as marked by the examiner) having a flat surface and extending from the main surface of said semiconductor substrate between said two trenches to said two isolation insulators;

an insulation film (7) extending from the upper surface of said floating electrode to a side surface of said floating electrode overlying said isolation insulator; and

a control gate (8) disposed on said insulation film to extend from the upper surface of said floating electrode to the side surface of said floating electrode.

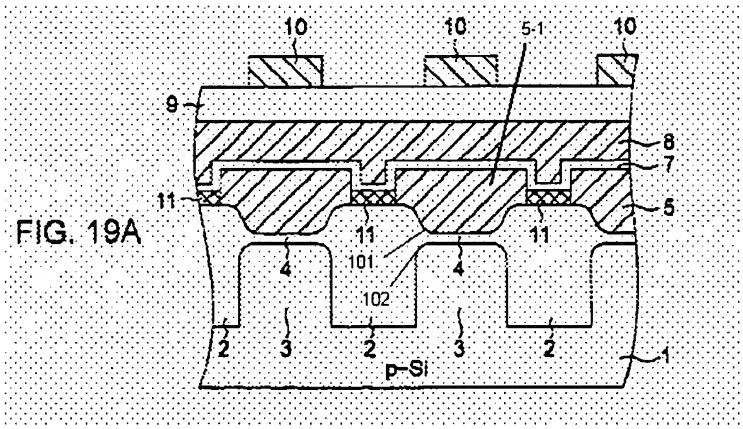

FIG. 19A

Referring to **claim 2**, Shimizu further discloses that a sidewall surface of said trench and the main surface of said semiconductor substrate underling said floating electrode are connected together by a portion (102, as marked by the examiner) providing said semiconductor substrate with a curved surface.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 3** is rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu et al. in view of Tseng U.S. Patent 6,413,836.

Shimizu discloses a non-volatile semiconductor memory device as claimed and as detailed above including trenches defined by trench isolation insulators (2) but fails to disclose that the trench has a width smaller than a distance between the two trenches (which is a length of the active region underlying the floating electrode) when seen in a direction of a length of the floating electrode. In other words, Shimizu fails to disclose that the width of the trench is smaller than a minimum feature size (a feature such as the active region in the instant case), the so-called lithographical limit in semiconductor processing. Tseng, in disclosing a method of making an isolation trench structure in a semiconductor substrate, teaches that when using a sacrificial spacer, the isolation trench can be made narrower beyond lithography limit (column 2, lines 18-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time

the invention was made to use a sacrificial spacer in forming the trenches of Shimizu. One would have been motivated to make such a modification in view of the Tseng's teachings that in forming trenches, using a sacrificial spacer allows the isolation trench to be narrower than the lithography limit, which defines a minimum feature size, such as a length of an active region or the distance between two adjacent trenches.

6. **Claim 4** is rejected under 35 U.S.C. §103(a) as being unpatentable over Shimizu et al. in view of Nishioka et al. U.S. Patent 5,994,733.

Shimizu discloses a non-volatile semiconductor memory device as claimed and as detailed above, wherein said semiconductor substrate (1) including a memory cell region having formed therein a memory cell including said floating electrode, said insulation film and said control electrode, and a peripheral circuitry region (Figs. 21A, 21B, and column 21, lines 53-60) corresponding to a region other than said memory cell region, in said peripheral circuitry region said semiconductor substrate (1) having the main surface provided with another trench (defined also by insulator 2), the non-volatile semiconductor memory device further comprising another isolation insulator (2) disposed in said another trench; but fails to disclose that, as seen in a direction substantially perpendicular to the main surface of said semiconductor substrate, said another isolation insulator arranged in said peripheral circuitry region is larger in thickness than said isolation insulator arranged in said memory cell region.

Nishioka et al., in disclosing a non-volatile semiconductor memory device (a flash memory device), teaches in column 8, lines 27-30, that the voltage resistance required in the

memory region is generally lower than that of the peripheral region and therefore the trenches can be relatively reduced in depth.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory device of Shimizu such that the isolation insulator arranged in the peripheral circuitry region is larger in thickness than the isolation insulator arranged in the memory cell region. One would have been motivated to make such a modification in view of the Nishioka's teachings that since voltage resistance required in the memory cell region is lower than that of the peripheral circuitry region, trench depth in the memory region can be smaller than that of the peripheral circuitry region, hence, trench depth in the peripheral circuitry region can be larger than that of the memory cell region.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
July 30, 2004